Abstract of the Disclosure

A time:space:time switch fabric incorporating an odd integer number of spatially distributed data switches and a plurality of spatially distributed data serializers. Each data switch has a first plurality of ingress ports, an equal plurality of egress ports, and a space switch for selectably interconnecting any one of the ingress ports to any one of the egress ports. Each data serializer has an input bus for receiving signals to be routed through the switch fabric, an output bus for outputting signals routed through the switch fabric, a plurality of egress ports selectably connectible to any one of the data switch ingress ports, and an equal plurality of ingress ports selectably connectible to any one of the data switch egress ports. The ingress/egress ports are characterized by:

(A) *p* planes, where *p* is a power-of-two integer less than or equal to the number of data serializer ingress and egress ports;

(B) *s* stages, where *s* is an odd integer number; and,

(C) a depth *d*, where *d* is a power-of-two integer less than or equal to the number of data switch ingress and egress ports.